Design and Evaluation of Physical Unclonable Function for Inorganic Printed Electronics

Ahmet Turan Erozan*, Mohammad Saber Golanbari*, Rajendra Bishnoi*,
Jasmin Aghassi-Hagmann*† and Mehdi B. Tahoori*
*Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany,
†Offenburg University of Applied Sciences, Offenburg, Germany
Email: {ahmet.erozan, golanbari, rajendra.bishnoi, jasmin.aghassi, mehdi.tahoori}@kit.edu

***Abstract*—Printed Electronics (PE) is a promising technology that provides mechanical flexibility and low-cost fabrication. These features make PE the key enabler for emerging applications, such as smart sensors, wearables, and Internet of Things (IoTs). Since these applications need secure communication and/or authentication, it is vital to utilize security primitives for cryptographic key and identification. Physical Unclonable Functions (PUF) have been adopted widely to provide the secure keys. In this work, we present a weak PUF based on Electrolyte-gated FETs using inorganic inkjet printed electronics. A comprehensive analysis framework including Monte Carlo simulations based on real device measurements is developed to evaluate the proposed PE-PUF. Moreover, a multi-bit PE-PUF design is proposed to optimize area usage. The analysis results show that the PE-PUF has ideal uniqueness, good reliability, and can operates at low voltage which is critical for low-power PE applications. In addition, the proposed multi-bit PE-PUF reduces the area usage around 30%.**

***Keywords*—Printed Electronics, Physical Unclonable Function, Security, Low-power, Emerging technologies, Electrolyte-gated transistors, Process variation, Multi-bit PUF.**

I. Introduction

Printed Electronics (PE) has become a promising technology in recent years since it provides mechanical flexibility, extreme low-cost and on-demand fabrication [1], which are superior features to traditional silicon-based counterparts. These features lead to broad application areas of PE, such as IoTs [2], wearables [3], radio frequency identification tags (RFIDs) [4], smart sensors [5], smart cards [6], smart labels [7] and photovoltaic cells [8].

In contrast to subtractive lithography-based manufacturing processes used in silicon-based electronics, PE circuits are formed by additive processes which place organic or inorganic materials on the top of various substrates. Organic-based printed transistors have been proposed to enable intelligent printed circuits [9],[10]. However, since they operate at high supply voltage (more than 10 V), they are not suitable for low-power applications. Electrolyte-gated Field Effect Transistors (EGFETs) based on inorganic materials have been developed to form low-power printed circuits since the EGFETs have high field-effect mobility and operates at low voltages (less than 1 V) [11],[12],[13].

The envisioned applications for PE require secure communication and/or authentication, for which secret keys are required [14],[4],[6],[7]. Physical Unclonable Functions (PUFs) have been proposed to provide such secret keys [15], which derive unpredictable keys from uncontrolled physical feature disorders [16],[17]. A PUF operates as a black box which accepts challenge input(s) and returns response output(s). PUFs are generally categorized as weak and strong PUFs, based on the number of challenge-response pairs (CRPs). Weak PUFs provide keys for cryptographic operations while strong PUFs are used for authentication [15].

Recently, one study has presented a strong PUF using organic materials to provide secret keys in PE [18]. The organic PUF generates a key based on the frequency difference of ring oscillators (RO). However, the organic PUF suffers from a high circuit complexity rendering it very vulnerable to yield problems and high operation voltage, which are unsuitable features for the low-power IOT applications.

In this paper, we propose an EGFET-based weak printed electronics-PUF (PE-PUF), which operates at low-voltage and has low circuit complexity. The proposed PE-PUF is a memory-based circuit that benefits from positive feedback created by two cross-coupled inverters to provide the output (response), and includes a control transistor enabling the circuit by an input signal (challenge). To evaluate the proposed PUF, we have developed a Monte Carlo based analysis framework including variation models based on the real EGFET measurements. Results obtained from our analysis framework show that the proposed PE-PUF has near to ideal uniqueness (50.1%) and good enough reliability (89%). Moreover, a multi-bit PE-PUF design is proposed to reduce the area usage for multiple bit key generation. The proposed multi-bit PE-PUF saves 31.02% area for 16-bit key with nearly ideal uniqueness (49.8%) and good reliability (92.6%). The summary of the contributions of this work is as follows:

- We present an EGFET based PE-PUF.
- We have generated a variation model of EGFET by using measurements from several fabricated EGFETs.
- We develop an analysis framework that includes Monte Carlo simulation flow for PE-PUF.
- We propose a multi-bit PE-PUF which is optimized to reduce area usage for multiple bits.

The rest of the paper is organized as follows. The background information is given in Section II. Section III explains the proposed PE-PUF designs. In Section IV, the analysis

framework for PE-PUF is described. Section V shows the simulation results, and in Section VI, the paper is concluded.

II. Background

A. Electrolyte-Gated Field Effect Transistors

Printed electronics is a complementary technology of conventional silicon-based electronics since it does not compete with it in terms of performance, integration density, and area. However, it enables flexible, on demand, and extreme low-cost fabrication, which are required in emerging applications, such as IoT, thanks to its materials and simple fabrication methods.

PE circuits are manufactured by using the variety of mask-free additive processes while conventional silicon-based technologies use comprehensive subtractive processes. Screen printing, flexography printing, offset printing, gravure printing, and inkjet printing are the fabrication methods that PE uses [2]. Various materials are placed on top of the flexible substrates to form PE circuits in these processes.

There are several types of printed transistors, which are composed of different materials to create functional PE circuits, such as organic-based thin film transistors (OTFTs) [10], and organic field-effect transistors (OFETs) [9]. However, these transistors require high supply voltage (>10 V) which is not suitable for low-power applications.

The EGFET has been proposed to provide low voltage operation [12]. Figure 1 illustrates the structure and the fabrication process of the EGFET. The EGFETs are based on indium oxide (In_2O_3) channel which is inkjet printed between lithographic structured indium tin oxide (ITO) drain and source electrodes. The main benefit of the indium oxide channel is the high intrinsic mobility and thus resulting in EGFETs with high field-effect mobility values ($>= 100cm^2/Vs$) [11]. In a next step, the electrolyte is also inkjet printed on the top of the channel in a way that the whole channel is covered. Due to the fact that electrolytes provide high capacitance, EGFETs show gate-capacitance values in the range of $4F/cm^2$, allowing to reduce the supply voltages to values below 1.0 V [11]. As a last step, PEDOT:PSS is inkjet printed on the electrolyte as top-gate to reduce the inner resistance of the electrolyte and enhance the switching speed of the EGFETs [12].

It has been shown that with this transistor technology, it is possible to design high performable circuits with extremely low supply voltage (<= 1.0 V) [19]. So, these properties of the EGFET make it suitable for the low-power PE applications.

B. Physical Unclonable Functions

PUF has been presented to provide secret keys [20]. It derives digital signatures from intrinsic manufacturing process variations. The inherent variation makes signatures unpredictable. Thus the signatures can be used as a key for security and authentication.

PUF is a function that produces a response corresponding to the challenge it accepts [15]. Since the relation between challenges and responses is unpredictable, it is represented as a black box function with CRPs. PUFs are categorized as weak PUFs which provide few secret keys and are used for the key storage of cryptographic algorithms, and strong PUFs which provide numerous secret keys depending on their inputs and are used for authentication [15].

The PUF metrics such as uniqueness and reliability can be used to evaluate the performance of the PUFs. The uniqueness and reliability are calculated by using Fractional Hamming Distance (FHD) which is given in Equation 1.

$$FHD(A,B) = \frac{1}{N}\sum_{i=1}^{N}|A_i - B_i| \quad (1)$$

A and B denote two different bit array containing N bits while i denotes the bit index. FHD calculates the fraction of the bits which differs from A to B.

The uniqueness metric indicates how unique the responses of the PUFs are. It is obtained by calculating the FHD of every two PUF responses. The average of the uniqueness of an ideal PUF should be 50%. The reliability metric explains the stability of the PUF response in the presence of different environmental and noise conditions. It is obtained by calculating the FHD between the reference PUF response and the PUF response in different environmental and noise conditions. In ideal case, the reliability should be 100%.

III. Proposed Printed Electronics PUF

Since the PE applications are low-cost devices, it is important to use as few number of circuit elements while designing PE circuits. Additionally, from this particular technology point of view, although there are p-type EGFETs, the performance of p-type EGFETs is orders of magnitude lower than n-type EGFETs [19]. For this reason, instead of p-type EGFETs, resistors should be used for the pull-up network. Lastly, the manufacturing variation of EGFETs is high because of its multilayer structure and intrinsic non-deterministic nature in droplet-based inkjet printing. So, the PUF circuit should be designed in a way that exploits the high manufacturing variation of EGFETs.

To this end, we have utilized a memory-based circuit which satisfies the considerations mentioned above. Besides,

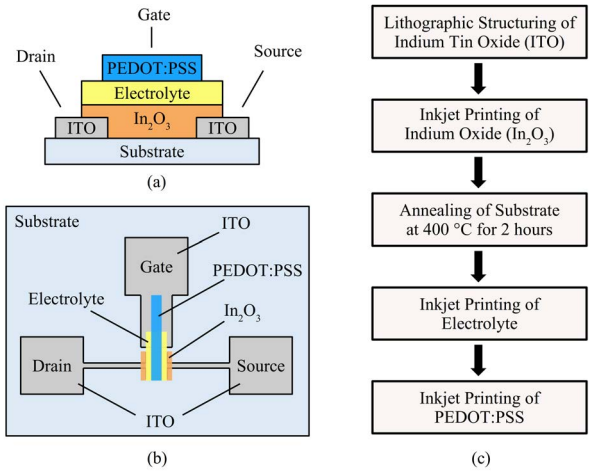

Fig. 1. a) Cross-sectional view of EGFET [12] b) Top view of EGFET [12] c) Fabrication process of EGFET

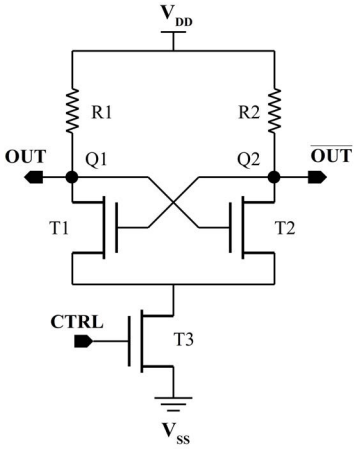

Fig. 2. The proposed single-bit PE-PUF circuit.

memory-based PUFs have nearly ideal average uniqueness results because of their working mechanism. Since we have also considered the usage of our PE-PUF for multi-bit design, area optimization through resource sharing is investigated. The details of the single-bit and multi-bit PE-PUF circuits are explained below.

A. Single-bit PE-PUF

The proposed memory-based PE-PUF is composed of two cross-coupled inverters and one control transistor to activate and deactivate the circuit. The schematic of the proposed PE-PUF is given in Figure 2.

The cross-coupled inverters create a positive feedback which forces the circuit to a stable state where the output is logic-0 or logic-1 depending on the manufacturing variation mismatch between inverter pairs. As an example, the timing diagram of the circuit to illustrate its working mechanism is given in Figure 3.

When control signal (CTRL) is logic-0, the $Q1$ and $Q2$ nodes are equal to V_{DD}. While the $CTRL$ is switching to logic-1, the feedback connections force the nodes to the stable states. Depending on the strength of the inverters, one node becomes logic-0 while the other becomes logic-1.

Figure 4 is the layout of the proposed PE-PUF circuit, which contains three EGFETs, two resistors, and five input/output pads which are V_{DD}, V_{SS}, $CTRL$, $Q1$, and $Q2$. Since our technology supports only one layer, the inverters are connected

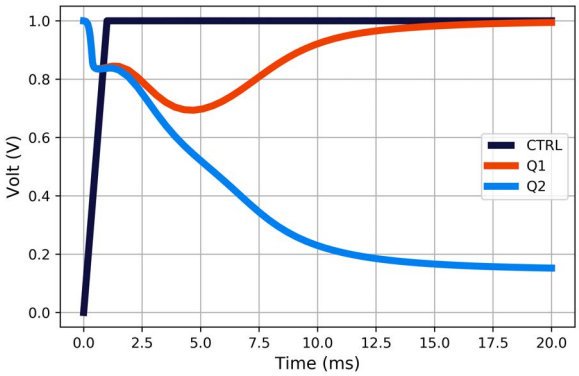

Fig. 3. An example timing diagram for single-bit PE-PUF circuit.

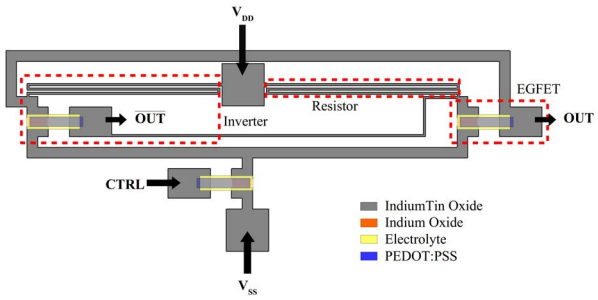

Fig. 4. The layout of the proposed single-bit PE-PUF circuit.

in a way that wires are not crossed. Moreover, the delays of the wires are designed to be equal.

B. Multi-bit PUF

Secret keys have multiple bits to be used in cryptographic algorithms and authentication. To obtain multi-bit keys, multiple single-bit PUF circuits can be used. However, simple replication of single-bit PUF circuits is inefficient as the increase of the area usage is proportional to the number of bits. There is a possibility to use one shared CTRL transistor for multiple single-bit PUF. However, since the current flowing through EGFET does not proportionally increase with the increase of the width, according to experimental results, the shared transistor, which flows equal current, uses the same area which separated transistors use. To reduce the area of multi-bit PUF circuit, resistors can be shared. Figure 5 illustrates the multi-bit PE-PUF design.

As shown in Figure 5, the resistors are shared among transistor pairs. For n bit array, n transistor pairs are required while the number of resistors is independent of the number of bits. Thus, resistor usage for multiple bits is reduced. After power-up, the control transistors of the transistor pairs are sequentially activated to generate multiple bits.

IV. Printed Electronics PUF Analysis Framework

In this section, the framework created to analyse the proposed PE-PUF circuit is explained. The models required for the PE-PUF analysis such as variation, thermal, and noise models are explained.

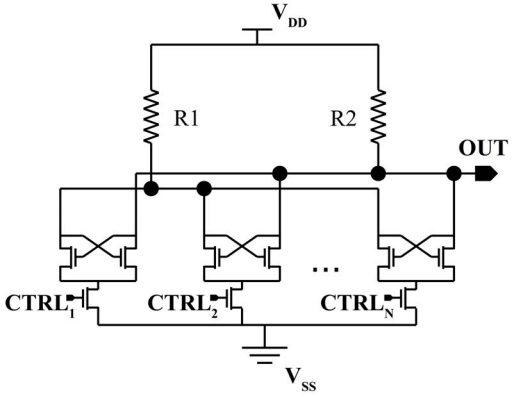

Fig. 5. The proposed multi-bit PUF circuit.

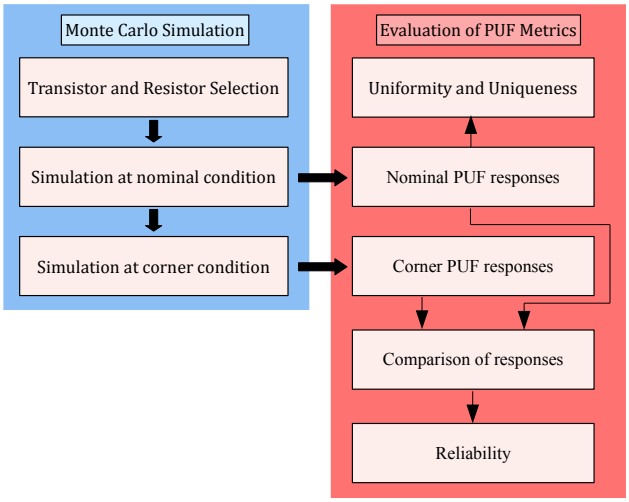

Fig. 6. The analysis flow of the proposed PE-PUF.

A. Overall PE-PUF Analysis Flow

Because of the fact that the behavior of a PUF circuit is based on manufacturing variations, it is critical to develop a variation aware simulation framework. For this reason, We have developed a Monte Carlo (MC) simulation flow, allowing to simulate the manufacturing variation for EGFET-based printed circuits, and integrated into a commercial EDA tool. In addition, an evaluation flow using MC simulation results to obtain the PUF metrics is established. Figure 6 illustrates the overall analysis flow of the printed PUF design.

The analysis flow is composed of the MC simulation and the evaluation parts of the PUF metrics. In the MC simulation, first, a set of PUF instances are created by selecting transistors and resistors among possible variation range. After that, PUF instances are simulated in nominal conditions and corner conditions.

The results obtained from the simulation in nominal conditions are used to calculate the uniqueness metrics and are compared with the results obtained from the simulation in corner conditions to calculate the reliability metric.

B. Variation Modelling

Since our PUF circuit is based on manufacturing variation, it is vital to have a variation model of the circuit elements. However, the EGFET does not have a variation model. So, we aimed to create EGFET variation model directly from the measurement data. Our approach is to create a binning model which includes the individual models of the numerous fabricated EGFETs and the variation effect can be simulated by making the individual models selectable. This approach not only allows us to develop a proper EGFET empirical variation model, but also enables us to use measurement data for more realistic PE-PUF analysis.

The model presented in [12] has the DC characteristics of the EGFET. It includes three equations for three regimes of the EGFET, namely below threshold, near threshold, and above threshold regimes. The below threshold regime is modelled by sub-threshold swing model [21] while the above threshold

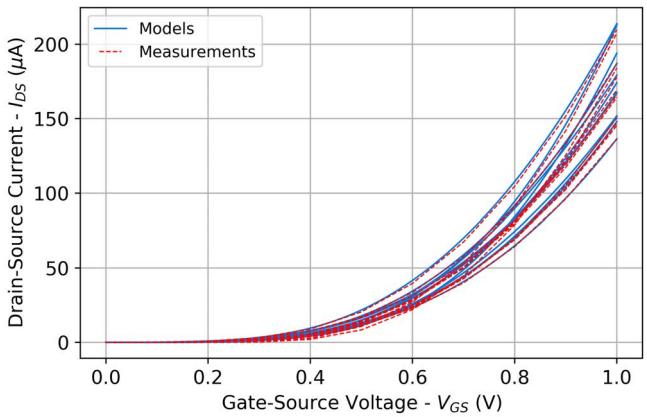

Fig. 7. The transfer curves (I_{DS}-V_{GS}) of the measurement and the model of EGFETs.

regime is modelled by a modified Curtice model [22]. The near threshold regime between the below and the above threshold regimes are interpolated by using third degree polynomial.

The boundaries of the near threshold regime are fixed in [12]. However, when the model is used to create individual models for various fabricated EGFETs under process variation, the fixed boundaries of the near threshold regime causes discontinuity and/or smoothness problem, creating convergence issues in simulation. The polynomial for the near threshold regime is given in Equation 2.

$$I_{DS} = aV_{gs}^3 + bV_{gs}^2 + cV_{gs} + d \tag{2}$$

where a, b, c and d denote the interpolation coefficients which are dependent on the boundaries of the near threshold regime. The polynomial and its slope must be monotonically increasing to provide continuity. To assure that, first and second derivatives of the polynomial which are given in Equation 3 and 4 must be positive.

$$\frac{\mathrm{d}I_{DS}}{\mathrm{d}V_{gs}} = 3aV_{gs}^2 + 2bV_{gs} + c \tag{3}$$

$$\frac{\mathrm{d}^2I_{DS}}{\mathrm{d}V_{gs}^2} = 6aV_{gs} + 2b \tag{4}$$

To obviate the discontinuity, we have developed a method which iteratively selects different boundaries for near threshold regimes for each transistor model to make sure that the first and second derivatives are positive. As a result, the fabricated EGFETs are modelled separately by changing the near threshold interval of the original EGFET model. Figure 7 shows the $I_{DS}-V_{GS}$ curves of the measurement and the model of several fabricated EGFETs. The models are implemented using Verilog-A and made it selectable. By changing model number, the variation of the EGFET is simulated.

C. Temperature and Noise Modeling

The results presented in [23] on the impact of temperature on EGFET characteristics are used to model the thermal effect. Since the saturated drain current $I_{d,sat}$ which is the combined result of other affected parameters is the circuit level

TABLE I
SATURATED DRAIN CURRENT RATIOS EXTRACTED FROM [23] FOR CORNER TEMPERATURES

Reference Temperature	Corner Temperature	Saturated Drain Current Ratio
23° C	60° C	1.2
23° C	-35° C	0.83

parameter, we directly use the saturated drain current to model the thermal effect.

The saturated drain current increases while the temperature is increasing from -35° C to 60° C. To create the thermal model for corner cases, highest ratios of the saturated drain current between 23° C and -35° C, and between 23° C and 60° C are calculated and given in Table I. The ratios are added to the variation model of the EGFET to be able to simulate the thermal effect on PUF circuit and obtain the reliability of the PUF circuit at corner temperature cases.

Since there is no noise analysis done for the EGFET, we used a method to model the noise effect on the circuit output. The method is that while CTRL transistor is turning on, a fixed amount of voltage (e.g., 8 mV) is added to one output (OUT) and subtracted from other output ($\overline{OUT}$), and vice versa. Therefore, the noise directly affects the response of the PE-PUF.

D. Extraction of PUF Metrics

The keys produced by the MC simulations are used to obtain the PUF metrics of the PE-PUF. The FHD between each key is calculated for the uniqueness. For reliability, the FHDs between the keys obtained in normal conditions and corner conditions are calculated.

V. RESULTS

A. Design Parameters

The PUF circuit is composed of three EGFETs and two resistors. The width and the length of the T1 and T2 EGFETs are selected as $100\mu m$ and $40\mu m$ respectively since these values are the parameters of the smallest fabricated EGFET. The width and the length of the T3 are $200\mu m$ and $40\mu m$ since T3 should be able to flow the sum of the current of T1 and T2.

The resistance values of R1 and R2 are selected in accordance with the reliability metric as it affects the reliability. So, the PUF circuits with different resistance values are simulated in nominal conditions and the conditions in which only noise is introduced. The reliability results for different resistance values are given in Figure 8.

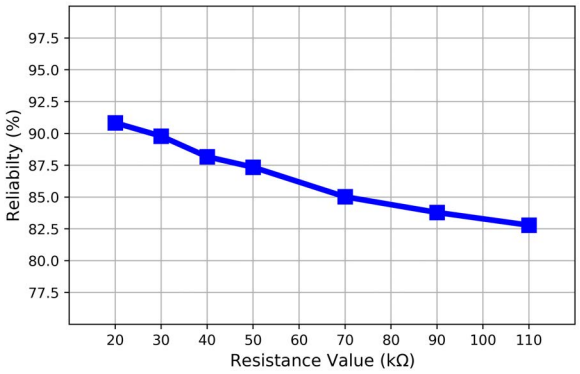

Fig. 8. Reliability results for different resistance values.

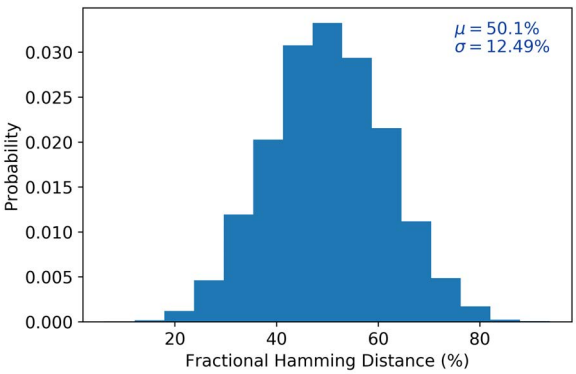

Fig. 9. Uniqueness of the proposed PE-PUF.

The results show that the smaller resistance value provide better reliability. Besides, the resistor area decreases while the resistance value is decreasing. However, while the resistance value decreases, the feedback strength of the inverters, which forces the PUF circuit to go to a stable state, also decreases. The low feedback strength of the inverters bring about unstable outputs. Therefore, the number of the unstable PUF outputs rapidly increases below 20 kΩ. For this reason, 20 kΩ is selected as resistance value to obtain better reliability, smaller area, and stable outputs.

B. PUF Metrics and Design Space Exploration

The analysis framework which is explained in Section IV is utilized to obtain the PUF metrics. More than 20,000 MC simulations were executed to obtain uniqueness and reliability metrics. Since the single-bit PUF circuit generates one bit, 16 single-bit PUF circuits are used to obtain 16-bit keys.

For uniqueness, 128x16-bit keys obtained in nominal condition, which denotes that temperature is 23° C, supply voltage is 1 V, and noise level is zero, are used. The histogram of the FHDs between keys is shown in Figure 9. The mean of the histogram should be ideally 50%. In our work, The mean and the standard deviation are 50.1% and 12.49%, respectively.

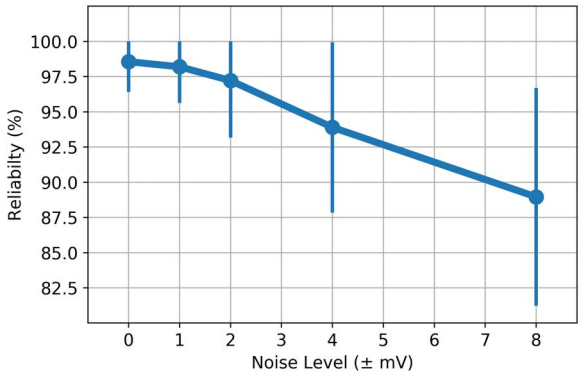

Fig. 10. Reliability of PE-PUF at different noise levels.

TABLE II
AREA USAGE AND SAVE OF THE CIRCUITS FOR VARIOUS NUMBER OF BITS.

# of Bit	Area Usage ($10^3 * pm^2$)		Area Save (%)
	Single-bit	Multi-bit	
1	272	272	0
2	544	454	16.54
4	1088	818	24.82
8	2176	1546	28.95
16	4352	3002	31.02

These results show that the uniqueness of our proposed PE-PUF is very close to the ideal uniqueness.

For reliability, the keys are obtained in nominal condition and corner condition, which denotes that temperature is 60° C, supply voltage is 1.1 V, and noise level is non-zero. The FHDs between the keys are calculated for reliability at different noise voltage levels and the FHD distributions are given in Figure 10. The results show that the worst reliability is around 89% where the noise level is $\pm 8\,mV$. In addition, the unreliability of the keys can be mitigated by error correction codes [16].

According to the mean and standard deviation of uniqueness histogram, the smallest FHD between two keys is 14.12% and the worst reliability is 89% which means the highest unreliability is 11%. Since the smallest uniqueness is greater than the highest unreliability, the keys are distinguishable in all cases.

Although multiple single-bit PUF circuit can be used to create multi-bit keys, a resource shared multi-bit PE-PUF circuit described earlier can be used to reduce the area usage. The area usage of the single-bit and the multi-bit PUF designs for various bit numbers, and the area reduction rates are given in Table II. The results show that the area usage can be reduced by 31.02% for 16-bit by using multi-bit PE-PUF circuit which has the same PUF metrics results.

The PUF metrics of the multi-bit PUF are obtained for 16-bit multi-bit circuit. The uniqueness of the multi-bit PE-PUF is 49.8%, which is near to the single-bit PE-PUF, since the circuit behaviour of one pair is same as the single-bit PE-PUF. However, the reliability of the multi-bit PE-PUF for $\pm 8mV$ noise is around 92.6%, which is higher than the single-bit PE-PUF since the leakage currents of the deactivated pairs reduce the effect of noise.

VI. CONCLUSION

Printed Electronics provides mechanical flexibility and low-cost fabrication which are crucial in many emerging applications, such as IoT, smart sensors, and wearables. These applications, however, require secret keys for secure communications and/or authentication. In this work, we addressed this requirement and proposed the PE-PUF based on electrolyte-gated inorganic inkjet printed transistors. We evaluated the performance of the PE-PUF by using the analysis framework based on real measurements of several printed transistors. We also proposed the multi-bit design of PE-PUF and optimized the area usage. The results show that the proposed PE-PUF has decent PUF metrics, and operates at low voltage ($1V$). Additionally, the optimized multi-bit design saves 31.02% area usage.

ACKNOWLEDGMENT

This work was supported by the Ministry of Science, Research and Arts of the state of Baden-Württemberg in form of the MERAGEM doctoral program.

REFERENCES

[1] J. S. Chang et al., "A Circuits and Systems Perspective of Organic/Printed Electronics: Review, Challenges, and Contemporary and Emerging Design Approaches," in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 7, no. 1, pp. 7-26, 2017.

[2] P. Rosa et al., "The potential of printed electronics and personal fabrication in driving the internet of things," Open J. Internet Things, vol. 1, no. 1, pp. 16-36, 2015.

[3] H. F. Castro et al., "Degradation of all-inkjet-printed organic thin-film transistors with TIPS-pentacene under processes applied in textile manufacturing," Organic Electronics, vol. 22, pp. 12-19, 2015.

[4] S. Zhang et al., "Research on smart sensing RFID tags under flexible substrates in printed electronics," in ICEPT, pp. 1006-1009, 2015.

[5] H. Marien et al., "Analog Organic ElectronicsBuilding Blocks for Organic Smart Sensor Systems on Foil," New York, NY, USA: Springer, 2012.

[6] J. Marques et al., "Thermoplastic packaging and embedding technology for ID-cards," in Proceedings of European Microelectronics Packaging Conference, pp. 1-5, 2013.

[7] L. W. F. Chaves, and C. Decker, "A survey on organic smart labels for the Internet-of-Things," in International Conference on Networked Sensing Systems, pp. 161-164, 2010.

[8] H. Youn et al., "Printed nanostructures for organic photovoltaic cells and solution-processed polymer light-emitting diodes," Energy Technology, vol. 3, no. 4, pp. 340-350, 2015.

[9] H. Sirringhaus, "25th Anniversary Article: Organic Field-Effect Transistors: The Path Beyond Amorphous Silicon," in Advanced Materials, pp. 1319-1335, 2014.

[10] K. Fukuda and S. Tokito, "Printed organic thin-film transistors," in Organic Electronics Materials and Devices, pp. 139-154, 2015.

[11] S. K. Garlapati et al., "Electrolyte-Gated, High Mobility Inorganic Oxide Transistors from Printed Metal Halides", ACS Appl. Mater. Interfaces, vol. 5, no. 22, pp. 11498-11502, 2013.

[12] G. C. Marques et al., "Electrolyte-Gated FETs Based on Oxide Semiconductors: Fabrication and Modeling," in IEEE Transactions on Electron Devices, vol. 64, no. 1, pp. 279-285, 2016.

[13] F. Rasheed et al., "A Smooth EKV-Based DC Model for Accurate Simulation of Printed Transistors and Their Process Variations," in IEEE Transactions on Electron Devices, vol. 65, no. 2, 2018.

[14] J. Lee et al., "A technique to build a secret key in integrated circuits for identification and authentication applications," in Symposium on VLSI Circuits, pp. 176-179, 2004.

[15] C. Herder et al., "Physical Unclonable Functions and Applications: A Tutorial," in Proceedings of the IEEE, vol. 102, no. 8, pp. 1126-1141, 2014.

[16] B. Gassend et al., "Silicon physical random functions," in Computer and Communications Security, pp. 148-160, 2002.

[17] U. Rhrmair et al., "Security based on physical unclonability and disorder," Book Chapter in Introduction to Hardware Security and Trust, 2011.

[18] K. Kuribara et al., "Organic physically unclonable function on flexible substrate operable at 2 V for IoT/IoE security applications," Organic Electronics, vol. 51, pp. 137-141, 2017.

[19] G. C. Marques et al., "Digital power and performance analysis of inkjet printed ring oscillators based on electrolyte-gated oxide electronics," in Applied Physics Letters, vol. 111, no. 10, 2017.

[20] M. Rostami et al., "Quo vadis, PUF?: Trends and challenges of emerging physical-disorder based security," in DATE, pp. 1-6, 2014.

[21] S. Sze and K. Ng, "Physics of Semiconductor Devices," Hoboken, NJ, USA: Wiley, 2006.

[22] W. R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," IEEE Trans. Microw. Theory Techn., vol. 17, no. 8, pp. 448-456, 1980.

[23] F. Seggern et al., "Temperature-Dependent Performance of Printed Field-Effect Transistors with Solid Polymer Electrolyte Gating," in ACS Applied Materials & Interfaces, vol. 8, no. 46, 2016.