# Call for Papers

# ISQED China 2014
# 16th International Symposium & Exhibits on

# QUALITY ELECTRONIC DESIGN

ISQED
2014 China Symposium
www.ISQED.org/china

## Oct. 27-29, 2014. Hangzhou, China

16th International Symposium on Quality Electronic Design (ISQED'14 China) is organized by the International Society for Quality Electronic Design with technical sponsorship from several IEEE Societies. This event is being sponsored by Hangzhou Dianzi University. The conference emphasizes innovations and the latest developments in System and IC Design, Sensors, MEMS & NEMS, Semiconductor Technology & Manufacturing, IC Packaging & PCB Technology, Test, and Bio & Nano Electronics. All past ISQED papers have been published in IEEE digital library Xplore and indexed by Scopus.

## Papers are accepted in the following areas

A pioneer and leading multidisciplinary conference, ISQED accepts and promotes papers in the following areas:

### Smart Sensors Design and Technology (SSDT)

Sensor and actuator devices for industrial use. Circuits and links for Sensor interfaces. Energy harvesting techniques. Device, circuit, and package level modeling of sensors. Networked sensors and data processing algorithms. Sensor fusion and sensor networks. Bio-sensors. Energy management in sensor chips. Sensors for robotics. Wireless sensor networks. Environmental sensors and sensors for ambient assisted living, for building automation, for automotive applications, and for aircraft. Underlying device technologies for sensors, such as MEMS, magnetic, etc. Touch screen sensors and capacitive vs. resistive sensing. Sensor Integration : Hardware & Software. Indoor positioning and navigation using MEMS sensors. MEMS microphones. Chemical sensors.

### Internet of Things (IoT), Technology, Design and Applications (IOT)

Mobile IoT. IoT Device or Circuit Design, IoT Applications and Services for Agriculture, Automotive, Civil & Industrial Infrastructure Monitoring, and Health Care. Architecture and Systems Design, Cloud Computing and Semantic web Technologies, Interface and Control Systems, IoT Analytics.

### System-level Design and Methodologies (SDM)

Emerging system-level design paradigms, methods and tools aiming at quality of systems including multi-core processors, embedded systems, and SoC. ESL design process and flow management. System-level design modeling, analysis, synthesis, and estimation for correct high-quality hardware/software systems. New concepts, methods and tools addressing the hardware and system design complexity and usage of technology information and manufacturing feedback in the system-, RTL- and logic level design. The influence of the nanometer technologies' issues on the system-, RTL- and logic-level design. System-level trade-off analysis and multi-objective (yield, power, delay, area …) optimization.

### Package and Three-Dimensional Integration (PTDI)

Architecture, circuit, package, and PCB/PWB design and effect on quality in emerging forms of vertical integration including 3D, 2.5D, multi-chip module, and any other innovating packaging techniques. Tools and methodologies dealing with electrical, stress, and thermal modeling and simulation for improved quality of product. Novel partitioning, power delivery design, clock tree design, heatsink/cooling methods, and design for test/yield techniques in vertically integrated circuits/chips. Design and technology solutions in system-on-chip versus system in a package (SiP) solutions. Die-package co-design and trade-off analysis.

### Integrated Circuit Design (ICD)

Low power circuits, memory, analog, RF, programmable logic, and FPGA circuits. Power-aware computing and communication. Design techniques and architecture for leakage current management, total power optimization, and power management. Low power interconnect solutions. Analog-to-digital and digital-to-analog converters. Robust SRAM cell and circuits. Effect of device and process reliability, robustness, and variation on the design of reliable circuits. Circuit design for reliability effects such as gate oxide integrity, electromigration, ESD, HCI, NBTI, PBTI etc.

### EDA Methodologies & IP Cores; Interoperability, Security, and Reuse (EDA)

EDA tools addressing management of design process, design flows and design databases. EDA tools interoperability issues and implications. Emerging EDA standards. EDA design methodologies and tools that address issues which impact the quality of the realization of designs into physical integrated circuits. IP modeling and abstraction. Design and maintenance of technology independent hard and soft IP blocks. Methods and tools for analysis, comparison and qualification of libraries and hard IP blocks. Challenges and solutions of the integration, testing, qualifying, and manufacturing of IP blocks from multiple vendors. Third party testing of IP blocks. Risk management of IP reuse. IP authoring tools and methodologies. Design for IP security. Novel techniques for IP water marking. Application of EDA tools to non-traditional problems such as smart power grid, Solar energy, etc.

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### Design Verification and Design for Testability (DVFT)

Hardware and software formal, assertion, and simulation based design verification techniques to ensure the functional correctness of hardware early in the design cycle. DFT and BIST for digital and SoC. DFT for analog/mixed-signal ICs and systems-on-chip, DFT/BIST for memories. Test synthesis and synthesis for testability. DFT economics, DFT case studies. DFT and ATE. Fault diagnosis, IDDQ test, novel test methods, effectiveness methods, fault models and ATPG, and DPPM prediction. SoC/IP testing strategies. Design methodologies dealing with the link between testability and manufacturing.

### Physical Design, Methodologies & Tools (PDM)

Physical design for manufacturing; Physical synthesis flows for correct-by-construction quality silicon, implementation of large SoC designs. Tool frameworks and data-models for tightly integrated incremental synthesis, placement, routing, and timing analysis. Placement, optimization, and routing techniques for noise sensitivity reduction and fixing. Algorithms and flows for harnessing crosstalk-delay during physical synthesis. Tool flows and techniques for antenna rule and electromigration rule avoidance and fixing. Spare-cell strategies for ECO, decoupling capacitance and antenna rule fixing. Reliable clock tree generation and clock distribution methodologies for Gigahertz designs. EDA tools, design techniques, and methodologies, dealing with issues such as: timing closure, R, L, C extraction, ground/Vdd bounce, signal noise/cross-talk /substrate noise, voltage drop, power rail integrity, electromigration, hot carriers, EOS/ESD, plasma induced damage and other yield limiting effects, high frequency effects, thermal effects, power estimation, and EMI/EMC.

### Emerging Process & Device Technologies and Design Issues (EDT)

Emerging processes & device technologies and implications on IC design with respect to design's time to market, yield, reliability, and quality. Emerging issues in DSM CMOS: e.g. sub-threshold leakage, gate leakage, technology road mapping and technology extrapolation techniques. New and novel technologies such as Double-Gate (DG)-MOSFET, FinFETs, strained CMOS, tunnel FETs, high-bandwidth metallization, carbon nanotubes, and nanodevices. Advanced SOI technologies such as trap-rich high-resistivity SOI, etc for wireless front-end SOC implementation. Device design and circuit optimization in emerging non-volatile memory and logic, such as Spin-Transfer Torque MRAM, Phase Change Memory, Resistive RAM, and memristors. Use of novel devices for cognitive computing.

### Design for Manufacturability/Yield & Quality (DFQ)

DFM/DFY/DFQ definitions, methodologies, matrices, and standards. Quality-based design methodologies and flows for custom, semi-custom, ASIC, FPGA, RF, memory, networking circuit, etc. Analysis, modeling, and abstraction of manufacturing process parameters and effects for highly predictable silicon performance. Design and synthesis of ICs considering factors such as: OPC, phase shifting, proximity correction, and sub-wavelength lithography, manufacturing yield and technology capability. Design for diagnosability, manufacturing defect detection and tolerance; self-diagnosis, calibration and repair. Design and manufacturability issues for digital, analog, mixed signal, RF, MEMS, opto-electronic, biochemical-electronic, and nanotechnology based ICs. Redundancy and other yield improving techniques. Global, social, and economic implications of design quality. Mask making methods and advances impacting manufacturability and yield.

### Antennas Technology, Design and Applications, Wireless Power Transfer (ATD)

## Submission of Papers

Paper submission must be done on-line through the conference web site at **www.isqed.org/china**. The guidelines for the final paper format are provided on the conference web site . Authors should submit FULL-LENGTH, original, unpublished papers (Minimum 4, maximum 8 pages) along with an abstract of about 200 words. To permit a **blind review**, **do not** include name(s) or affiliation(s) of the author(s) on the manuscript and abstract. The complete contact author information needs to be entered separately. Please check the as-printed appearance of your paper before sending your paper. In case of any problems email isqed2014_china@isqed.org. Please note the following important dates:

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| **Paper Submission Deadline** | **July 21, 2014** |
| Acceptance Notifications | Aug. 18, 2014 |
| Final Camera-Ready paper | Sept. 18, 2014 |

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